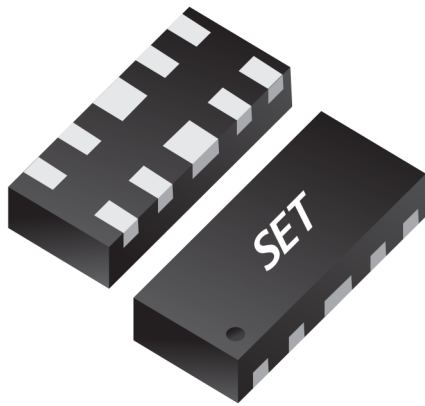


# ESD Protection Diodes

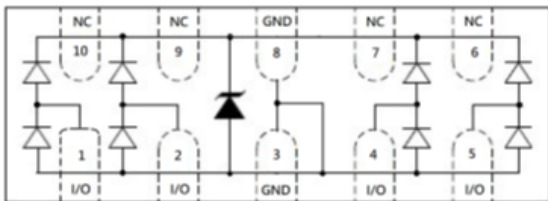
Ultra-Low Capacitance ESD and Transient Voltage Protection Array

SD0504F25U1

DFN2510



## Pinout and Functional Block Diagram



## Applications

- Serial ATA
- PCI Express
- Desktops, Servers and Notebooks
- MDDI Ports
- USB 2.0 / 3.0 Power and Data Line Protection
- Display Ports
- High Definition Multi-Media Interface (HDMI)
- Digital Visual Interface (DVI)

## Order Information

Type	Package	Marking	Size (mm)	Delivery Form	Delivery Quantity
SD0504F25U1	DFN 2510	0524P	2.5 x 1.0 x 0.5	7" T&R	3000 PCS

## Description

SD0504F25U1 is an ultra-low capacitance Transient Voltage Suppressor (TVS) designed to protection for high-speed data interfaces. With typical capacitance of 0.2 pF (I/O to I/O) only, SD0504F25U1 is designed to protect parasitic-sensitive systems against over-voltage and over-current transient events. It complies with IEC 61000-4-2 (ESD), Level 4(± 15 kV air, ± 8 kV contact discharge), IEC61000-4-4 (electrical fast transient-EFT) (40 A, 5 / 50 ns), very fast charged device model (CDM) ESD and cable discharge event (CDE), etc. SD0504F25U1 uses ultra-small DFN2510 package. Each SD0504F25U1 device can protect four high-speed data lines. The combined features of ultra-low capacitance, ultra-small size and high ESD robustness make SD0504F25U1 ideal for high-speed data ports and high-frequency lines (e.g., HDMI & DVI) applications. The low clamping voltage of the SD0504F25U1 guarantees a minimum stress on the protected IC.

## Features

- IEC61000-4-2 (ESD) ± 25 kV (Air), ± 20 kV (Contact)
- IEC61000-4-4 (EFT) 40 A (5 / 50 ns)
- Cable Discharge Event (CDE)
- Package Optimized for High-speed Lines
- Ultra-small Package(2.5 mm x 1.0 mm x 0.5 mm)
- Protects four data line
- Low capacitance: 0.2 pF (I/O to I/O)
- Low leakage current
- Low clamping voltage
- Each I/O pin can withstand over 1000 ESD strikes for ± 8 kV contact discharge
- Flammability Rating: UL 94 V-0
- Halogen free and RoHS compliant

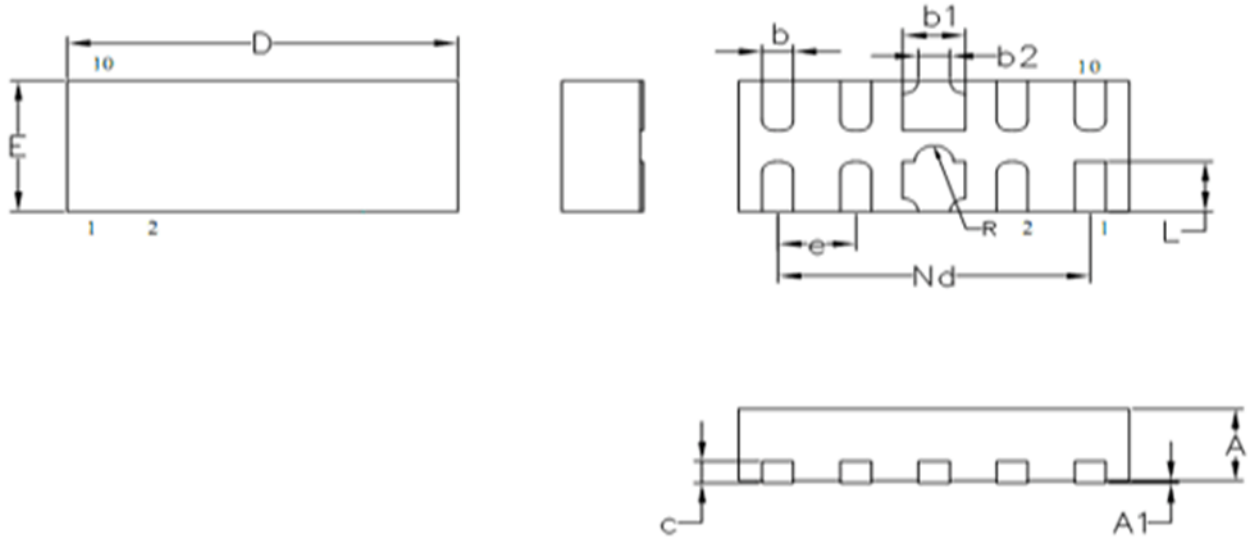
# ESD Protection Diodes

Ultra-Low Capacitance ESD and Transient Voltage Protection Array

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## Package Dimensions – DFN2510



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
D	2.45	2.55	0.096	0.100
E	0.95	1.05	0.037	0.041
b1	0.35	0.45	0.014	0.018
b2	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
L	0.33	0.43	0.013	0.017
Nd	2.00 BSC		0.079 BSC	
e	0.50 BSC		0.020 BSC	
R	0.10	0.15	0.004	0.006
A	0.45	0.55	0.018	0.022
c	0.15 REF		0.006 REF	
A1	0.00	0.05	0.000	0.002

# ESD Protection Diodes

Ultra-Low Capacitance ESD and Transient Voltage Protection Array

SD0504F25U1

DFN2510

## Limiting Values

( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{ESD}$	Electrostatic Discharge Voltage	IEC 61000-4-2; Contact Discharge	-	20	kV
		IEC 61000-4-2; Air Discharge	-	25	kV
$P_{PP}$	Peak Pulse Power (8 / 20 $\mu\text{s}$ )	-	-	60	W
$T_A$	Operating Temperature Range	-	-55	125	$^\circ\text{C}$
$T_{stg}$	Storage Temperature Range	-	-55	150	$^\circ\text{C}$

## Electrical Characteristics

( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit
$V_{RWM}$	Max. Reverse Working Voltage	Any I/O pin to GND	-	-	5.0	V
$V_{BR}$	Breakdown Voltage	$I_T = 1\text{ mA}$ Any I/O pin to GND	6.0	-	9.0	V
$I_R$	Reverse Leakage Current	$V_{RWM} = 5\text{ V}$ Any I/O pin to GND	-	-	1.0	$\mu\text{A}$
$V_C$	Clamping Voltage	$I_{PP}=1\text{ A}$ , $t_p=8 / 20\ \mu\text{s}$ Any I/O pin to GND	-	-	10	V
		$I_{PP}=4.0\text{ A}$ , $t_p=8 / 20\ \mu\text{s}$ Any I/O pin to GND	-	-	15	V
$C_1$	Parasitic Capacitance	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ Between I/O and GND	-	0.4	0.5	pF
$C_2$	Parasitic Capacitance	$V_R = 0\text{ V}$ , $f = 1\text{ MHz}$ Between I/O and I/O	-	0.2	0.3	pF

Note: I/O pins are pin 1,2,4,5, GND pins are pin 3,8.

# ESD Protection Diodes

Ultra-Low Capacitance ESD and Transient Voltage Protection Array

SD0504F25U1

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## Performance Curve for Reference

( $T_A=25\text{ }^\circ\text{C}$  unless otherwise noted)

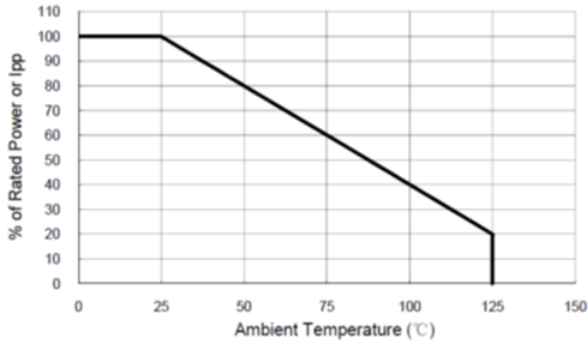


FIGURE 1  
Power Derating Curve

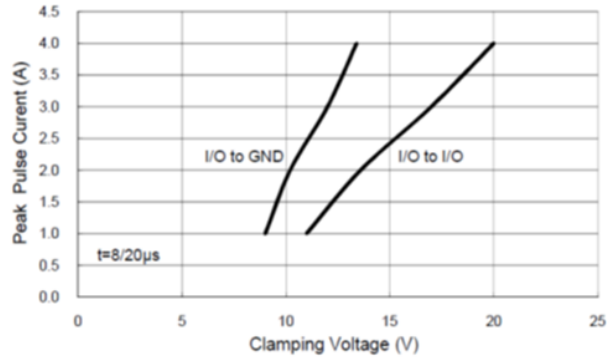


FIGURE 2  
Clamping Voltage VS. Peak Pulse Current

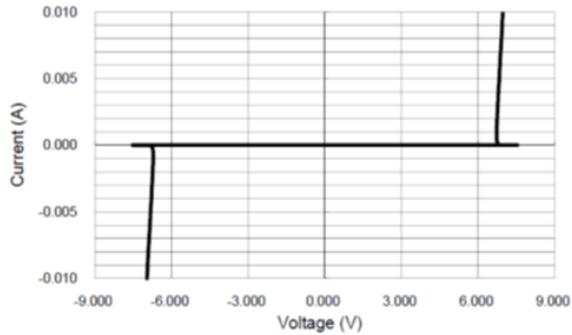


FIGURE 3  
Voltage Sweeping of I/O to I/O

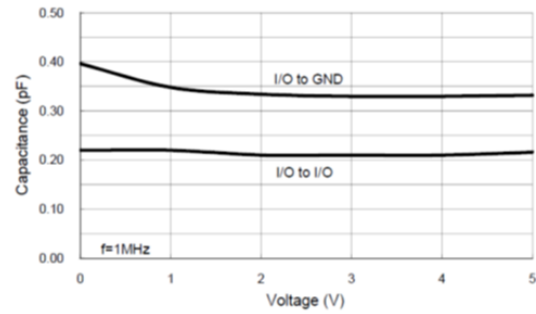


FIGURE 4  
Voltage VS. Capacitance

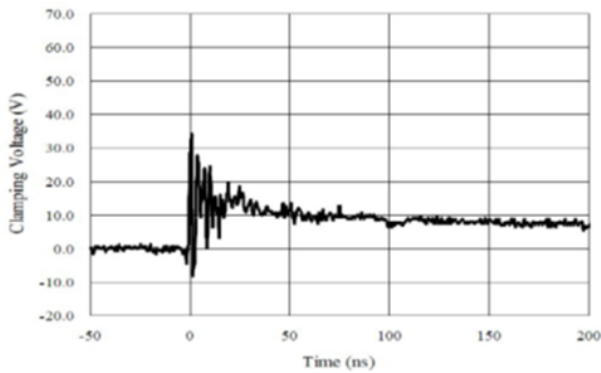


FIGURE 5  
ESD Clamping of I/O to GND  
(+8 kV Contact Per IEC 61000-4-2)

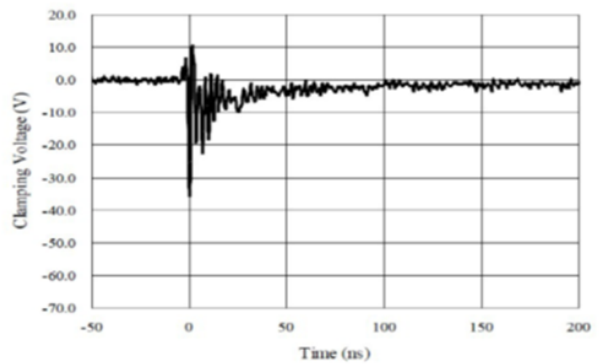


FIGURE 6  
ESD Clamping of I/O to GND  
(-8 kV Contact Per IEC 61000-4-2)

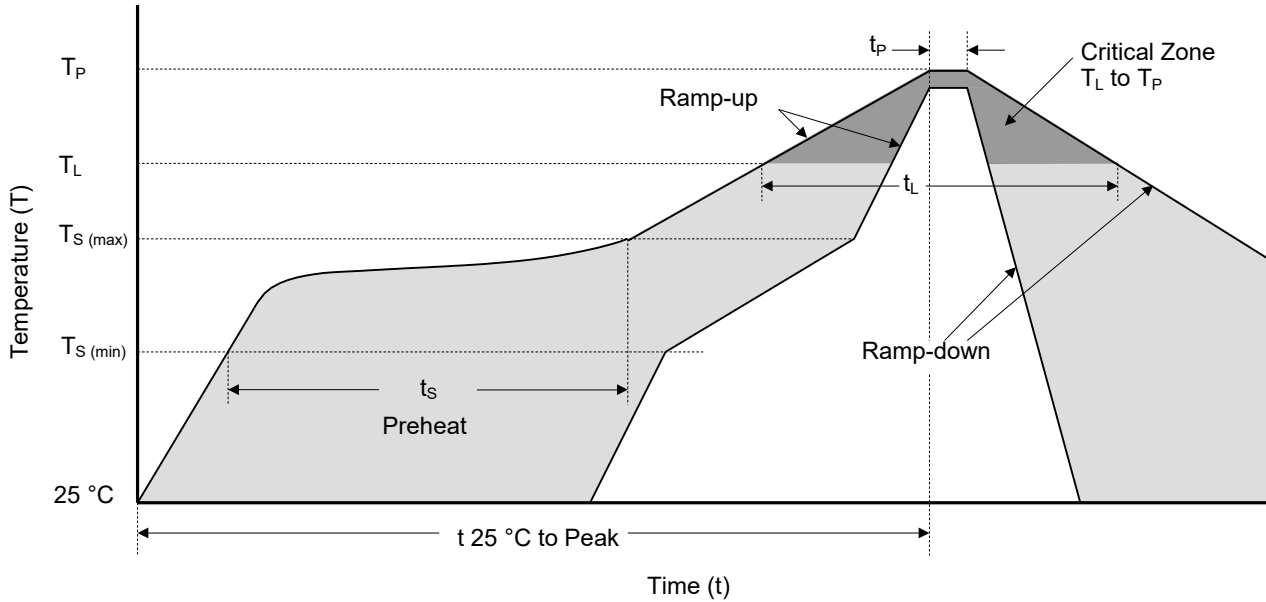
# ESD Protection Diodes

Ultra-Low Capacitance ESD and Transient Voltage Protection Array

SD0504F25U1

DFN2510

## Soldering Parameters



Reflowing Condition

Reflow Soldering Parameters		Lead-Free Assembly
Pre-heat	Temperature Min ( $T_{S(min)}$ )	150 °C
	Temperature Max ( $T_{S(max)}$ )	200 °C
	Time (min to max) ( $t_s$ )	60 ~ 120 seconds
Average Ramp Up Rate (Liquidus Temp ( $T_L$ ) to Peak)		3 °C / second max.
$T_{S(max)}$ to $T_L$ Ramp-up Rate		3 °C / second max.
Reflow	Temperature ( $T_L$ ) (Liquidus)	217 °C
	Time (min to max) ( $t_L$ )	60 ~ 150 seconds
Peak Temperature ( $T_P$ )		260 <sup>+0/-5</sup> °C
Time of within 5 °C of Actual Peak Temperature ( $t_p$ )		20 ~ 40 seconds
Ramp-down Rate		6 °C / second max.
Time from 25 °C to Peak Temperature		8 Minutes max.
Do Not Exceed		260 °C



# ATTENTION

## Usage

1. TVS must be operated in the specified ambient temp.
2. Do not clean the TVS with strong polar solvent such as ketone, esters, benzene and halogenated hydrocarbon, to avoid damaging the encapsulating layer.
3. Please do not apply severe vibration, shock or pressure to TVS, to avoid element cracking.

## Replacement

1. If TVS is visually damaged, please replace it.
2. TVS is a non-repairable product. For safety sake, please use equivalent TVS for replacement.

## Storage

1. Storage Temp. Range: (-55 to 150) °C.
2. Do not store the TVS at the high temp., high humidity or corrosive gas environment, to avoid influencing the solder-ability of the lead wires. The product shall be used up within 1 year after receiving the goods.

## Environmental Conditions

1. TVS should not be exposed to the open air, nor direct sunshine.
2. TVS should avoid rain, water vapor or other condition of high temp. and high humidity.
3. TVS should avoid sand dust, salt mist, or other harmful gases.

## Max. Typical Capacitance of TVS

The typical capacitance of TVS is listed in the specifications. Designers may refer to it when designing TVS in High frequency circuit.

## Installation Mechanical Stress

1. Do not knock TVS when installing, to avoid mechanical damage.
2. Please do not apply severe vibration, shock or pressure to TVS, to avoid surface resin or element cracking.

# ESD Protection Diodes













































Ultra-Low Capacitance ESD and Transient Voltage Protection Array

SETsafe

SET fuse

SD0504F25U1

DFN2510

Package Outline					Circuit Diagram					
										
DFN0603	DFN1006	DFN1006-3L	DFN1610	DFN2020-3L	1CH/UNI	1CH/BI	2CH/UNI	2CH/BI	1CH/BI	1CH/UNI
										
DFN1610-6L	DFN2010-8L	DFN2510	DFN2626-10L	DFN3810-9L	1CH/UNI	1CH/BI	1CH/UNI	1CH/BI	2CH/UNI	2CH/BI
										
SOD-923	SOD-523	SOD-323	SOD-123	SOT-143	1CH/UNI	2CH/UNI	2CH/UNI	4CH/UNI	5CH/UNI	4CH/UNI
										
SOT-523	SOT-323	SOT-23	SOT-363	SOT-23-6L	2CH/BI	4CH/UNI	4CH/UNI	8CH/UNI	8CH/UNI	8CH/UNI